AMENDMENTS TO THE CLAIMS

Please amend the claims as they currently stand so that they are in accord with the following listing of the claims:

1. (currently amended) A layer structure for Si-based bipolar transistors, comprising a semiconductor layer and an emitter layer formed over the semiconductor layer, wherein ~~locally~~ thin oxide and/or nitride layers are formed locally between the semiconductor layer and the emitter layer, characterized in that the emitter layer adjoining the semiconductor layer has a monocrystalline region and, separated from the semiconductor layer by the monocrystalline region, a polycrystalline or amorphous region.

2. (currently amended) The layer structure as set forth in claim 1 ~~characterized in that~~ wherein the semiconductor layer comprises an $Si_xGe_yC_{1-x-y}$-cover layer, an Si-buffer layer and a silicon substrate with the parameters x, y in the range $0 \leq x, y \leq 1$.

3. (previously presented) The layer structure as set forth in claim 2, comprising an electrically active zone of which at least a part is formed in the $Si_xGe_yC_{1-x-y}$-cover layer.

4. (currently amended) The layer structure as set forth in claim 1 ~~characterized in that~~ wherein an oxygen contamination is present at an interface between the emitter layer and the semiconductor layer, the oxygen contamination having an oxygen amount of less than 1×10^{15} cm^{-2}.

5. (currently amended) A process for producing a layer structure for ~~an~~ Si-based bipolar transistor, said process comprising the steps of:

pre-treating ~~the~~ a surface of ~~the~~ a silicon substrate with hydrofluoride-bearing solvents;

storing the ~~samples~~ substrate thereafter for less than one hour prior to introduction into a CVD reactor~~;~~;

pre-tempering ~~of~~ the ~~samples~~ substrate in the temperature range of 650 °C – 1100 °C in hydrogen-bearing gases with tempering times in the range ~~of~~ between 5 seconds and 120 minutes~~;~~;

supplying a doping gas during cooling to ~~the~~ a layer growth temperature~~;~~; and

applying a partially monocrystalline emitter layer with the addition of silane and doping gas at a temperature in the range 450 - 700°C, such that the emitter layer initially grows in monocrystalline form and then changes into a polycrystalline and/or amorphous layer.

6. (currently amended) The process of claim 5, wherein the step of applying the partially monocrystalline emitter layer is accomplished by chemical ~~gas~~ vapor phase deposition at low pressure in a multi-wafer reactor.

7. (previously presented) The process of claim 5, wherein the partially monocrystalline emitter layer is formed by a doped $Si_xGe_yC_{1-x-y}$-cover layer with the parameters x, y in the range $0 \leq x, y \leq 1$.

8. (currently amended) The process of claim 5, further comprising the step of:

subjecting the ~~samples~~ substrate to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold without introducing air into ~~the~~ a CVD Installation prior to the pre-tempering step ~~Operation~~, in hydrogen-bearing gases.

9. (currently amended) The process of claim 5, further comprising the step of:

subjecting the layer structure to further technological sub-steps after forming a Si-cover layer and before depositing the partially monocrystalline emitter layer, ~~such as for example~~ said sub-steps chosen from the list of an oxidation procedure, an implantation procedures, an etching procedures and masking sub-steps~~, after forming the Si cover layer and before depositing the partially crystalline emitter layer~~.

10. (cancelled)

11. (currently amended) The process of claim 5, wherein ~~the~~ a doping element for the partially monocrystalline emitter layer comprises arsenic.

12. (currently amended) The process of claim 5, further comprising the step of:

introducing at least one emitter dopant during ~~the~~ a CVD deposition procedure for growth of the emitter layer.

13. (currently amended) The process of claim 5, further comprising the step of:

introducing ~~the~~ an emitter dopant in the cooling ~~down process~~ step and prior to the addition of silane for growth of the partially monocrystalline emitter layer.

14. (previously presented) The process of claim 5, further comprising the step of:

depositing a homogeneously doped partially monocrystalline emitter layer or alternately depositing, to increase the growth rate, doped and undoped regions of the partially monocrystalline emitter layer.

15. (previously presented) The process of claim 5, further comprising the step of:

applying the partially monocrystalline emitter layer to Si-substrate wafers.

16. (currently amended) The process of claim 5, further comprising the step of:

applying the partially monocrystalline emitter layer to commercial Si-substrate wafers or commercial 'silicon-on-insulator' (SOI)-wafers ~~and~~ or Si-wafers with homo-epitaxial layers and Si-collector structures and Si-base structures ~~formed in accordance with the state of the art~~.

17. (currently amended) The process of claim 5, wherein the partially monocrystalline emitter layer is used in ~~the~~ a heterostructure of the type Si-emitter/Si/Si_yC_{1-y}/Si-substrate.

18. (currently amended) The process of claim 5, wherein the partially monocrystalline emitter layer is used in a three-component material system of the kind Si-emitter/Si/$Si_xGe_yC_{1-x-y}$, $Si_xGe_yO_{1-x-y}$, with the parameters x, y in the range $0 \leq x, y \leq 1$, on Si-substrates.

19. (previously presented) The process of claim 6, wherein the partially monocrystalline emitter layer is formed by a doped $Si_xGe_yC_{1-x-y}$-cover layer with the parameters x, y in the range $0 \leq x, y \leq 1$.

20. (currently amended) The process of claim 7, further comprising the step of:

subjecting the ~~samples~~ substrate to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold without introducing air into ~~the~~ a CVD Installation prior to the pre-tempering step ~~operation~~, in hydrogen-bearing gases.

21. (currently amended) The process of claim 19, further comprising the step of:

subjecting the ~~samples~~ substrate to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold without introducing air into ~~the~~ a CVD Installation prior to the pre-tempering step ~~operation~~, in hydrogen-bearing gases.

22. (currently amended) The process of claim 6, further comprising the step of:

subjecting the ~~samples~~ substrate to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold without introducing air into ~~the~~ a CVD installation prior to the pre-tempering step ~~operation~~, in hydrogen-bearing gases.

23. (currently amended) The process of claim 8, further comprising the step of:

subjecting the layer structure to further technological sub-steps after forming a Si-cover layer and before depositing the partially monocrystalline emitter layer ~~such as for example~~ said sub-steps chosen from the list of an oxidation procedures, an implantation procedures, an etching procedures and masking sub-steps~~, after forming the Si-cover layer and before depositing the partially crystalline emitter layer~~.

24. (currently amended) The process of claim 20, further comprising the step of:

subjecting the layer structure to further technological sub-steps after forming a Si-cover layer and before depositing the partially monocrystalline emitter layer ~~such as for example~~ said sub-steps chosen from the list of an oxidation procedures, an implantation procedures, an etching procedures and masking sub-steps~~, after forming Si-cover layer and before depositing the partially crystalline emitter layer~~.

25. (currently amended) The process of claim 21, further comprising the step of:

subjecting the layer structure to further technological sub-steps after forming a Si-cover layer and before depositing the partially monocrystalline emitter layer ~~such as for example~~ said sub-steps chosen from the list of an oxidation procedures, an implantation procedures, an etching procedures and masking sub-steps~~, after forming the Si-cover layer and before depositing the partially crystalline emitter layer~~.

26. (currently amended) The process of claim 22, further comprising the step of:

subjecting the layer structure to further technological sub-steps after forming a Si-cover layer and before depositing the partially monocrystalline emitter layer ~~such as for example~~ said sub-steps chosen from the list of an oxidation procedures, an implantation procedures, an etching procedures and masking sub-steps~~, after forming the Si-cover layer and before depositing the partially crystalline emitter layer~~.

27. (cancelled)

28. (cancelled)

29. (cancelled)

30. (cancelled)

31. (cancelled)

32. (currently amended) The process of claim 5, wherein ~~the~~ a doping element for the partially monocrystalline emitter layer comprises phosphorus.

33. (new) A layer structure for Si-based bipolar transistors, comprising a semiconductor layer and an emitter layer formed over the semiconductor layer, wherein thin oxide and/or nitride layers are formed locally between the semiconductor layer and the emitter layer, characterized in that the emitter layer adjoining the semiconductor layer is a mono-crystalline Silicon layer up to an end of the emitter layer.

34. (new) The layer structure as set forth in claim 33 wherein the semiconductor layer comprises a $Si_xGe_yC_{1-x-y}$-cover layer, a Si-buffer layer and a silicon substrate with the parameters x, y in the range $0 \leq x, y \leq 1$.

35. (new) The layer structure as set forth in claim 34, comprising an electrically active zone of which at least a part is formed in the $Si_xGe_yC_{1-x-y}$-cover layer.

36. (new) The layer structure as set forth in claim 33 wherein an oxygen contamination is present at an interface between the emitter layer and the semiconductor layer, the oxygen contamination having an oxygen amount of less than 1×10^{15} cm^{-2}.

37. (new) A process for producing a layer structure for a Si-based bipolar transistor, said process comprising the steps of:

pre-treating a surface of a silicon substrate with hydrofluoride-bearing solvents;

storing the substrate thereafter for less than one hour prior to introduction into a CVD reactor;

pre-tempering the substrate in the temperature range of 650 °C – 1100 °C in hydrogen-bearing gases with tempering times in the range between 5 seconds and 120 minutes;

supplying a doping gas during cooling to a layer growth temperature; and

applying a monocrystalline emitter layer with the addition of silane and a doping gas at a temperature in the range 450 - 700°C, such that an initial monocrystalline growth of the Si-emitter layer is maintained up to an end of the layer deposition.

38. (new) The process of claim 37, wherein the step of applying the monocrystalline emitter layer is accomplished by chemical vapor phase deposition at low pressure in a multi-wafer reactor.

39. (new) The process of claim 37, wherein the monocrystalline emitter layer is formed by a doped $Si_xGe_yC_{1-x-y}$-cover layer with the parameters x, y in the range $0 \leq x, y \leq 1$.

40. (new) The process of claim 37, further comprising the step of:

subjecting the substrate to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold without introducing air into a CVD Installation prior to the pre-tempering step, in hydrogen-bearing gases.

41. (new) The process of claim 37, further comprising the step of:

subjecting the layer structure to further technological sub-steps after forming a Si-cover layer and before depositing the monocrystalline emitter layer, said sub-steps chosen from the list of an oxidation procedure, an implantation procedures, an etching procedures and masking sub-steps.

42. (new) The process of claim 37, wherein a doping element for the monocrystalline emitter layer comprises arsenic.

43. (new) The process of claim 37, further comprising the step of:

introducing at least one emitter dopant during a CVD deposition procedure for growth of the emitter layer.

44. (new) The process of claim 37, further comprising the step of:

introducing an emitter dopant in the cooling step and prior to the addition of silane for growth of the monocrystalline emitter layer.

45. (new) The process of claim 37, further comprising the step of:

depositing a homogeneously doped monocrystalline emitter layer or alternately depositing, to increase the growth rate, doped and undoped regions of the monocrystalline emitter layer.

46. (new) The process of claim 37, further comprising the step of:

applying the monocrystalline emitter layer to Si-substrate wafers.

47. (new) The process of claim 37, further comprising the step of:

applying the monocrystalline emitter layer to commercial Si-substrate wafers or commercial 'silicon-on-insulator' (SOI)-wafers or Si-wafers with homo-epitaxial layers and Si-collector structures and Si-base structures.

48. (new) The process of claim 37, wherein the monocrystalline emitter layer is used in a heterostructure of the type Si-emitter/Si/Si_yC_{1-y}/Si-substrate.

49. (new) The process of claim 37, wherein the monocrystalline emitter layer is used in a three-component material system of the kind Si-emitter/Si/$Si_xGe_yC_{1-x-y}$, $Si_xGe_yO_{1-x-y}$, with the parameters x, y in the range $0 \leq x, y \leq 1$, on Si-substrates.

50. (new) The process of claim 38, wherein the monocrystalline emitter layer is formed by a doped $Si_xGe_yC_{1-x-y}$-cover layer with the parameters x, y in the range $0 \leq x, y \leq 1$.

51. (new) The process of claim 39, further comprising the step of:

subjecting the substrate to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold without introducing air into a CVD Installation prior to the pre-tempering step, in hydrogen-bearing gases.

52. (new) The process of claim 50, further comprising the step of:

subjecting the substrate to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold without introducing air into a CVD Installation prior to the pre-tempering step, in hydrogen-bearing gases.

53. (new) The process of claim 38, further comprising the step of:

subjecting the substrate to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold without introducing air into a CVD installation prior to the pre-tempering step, in hydrogen-bearing gases.

54. (new) The process of claim 40, further comprising the step of:

subjecting the layer structure to further technological sub-steps after forming a Si-cover layer and before depositing the monocrystalline emitter layer said sub-steps chosen from the list of an oxidation procedure, an implantation procedure, an etching procedure and masking sub-steps.

55. (new) The process of claim 51, further comprising the step of:

subjecting the layer structure to further technological sub-steps after forming a Si-cover layer and before depositing the monocrystalline emitter layer said sub-steps chosen from the list of an oxidation procedure, an implantation procedure, an etching procedure and masking sub-steps.

56. (new) The process of claim 52, further comprising the step of:

subjecting the layer structure to further technological sub-steps after forming a Si-cover layer and before depositing the monocrystalline emitter layer said sub-steps chosen from the list of an oxidation procedure, an implantation procedure, an etching procedure and masking sub-steps.

57. (new) The process of claim 53, further comprising the step of:

subjecting the layer structure to further technological sub-steps after forming a Si-cover layer and before depositing the monocrystalline emitter layer said sub-steps chosen from the list of an oxidation procedure, an implantation procedure, an etching procedures and masking sub-steps.

58. (new) The process of claim 37, wherein a doping element for the monocrystalline emitter layer comprises phosphorus.